CLAIMS

What is claimed is:

1. An integrated circuit device comprising:
an array of cells, said cells comprising a source, a drain and a gate;
a common source line coupled with said source; and
a source contact disposed outside of said common source line and coupled with said source.

2. The integrated circuit device of Claim 1 comprising substantially straight word lines.

3. The integrated circuit device of Claim 1 wherein said common source line has a substantially uniform width within said array of cells.

4. The integrated circuit device of Claim 1 wherein said source contact is disposed in a row with drain contacts.

5. The integrated circuit device of Claim 1 wherein said source contact is coupled to said common source line under a gate structure.

6. The integrated circuit device of Claim 1 wherein said integrated circuit device comprises non-volatile memory.

7. The integrated circuit device of Claim 6 wherein said non-volatile memory comprises a floating gate as a charge storage element.

8. An integrated circuit device wherein a first region under a gate comprises overlapping lateral diffusions of source and drain implantation regions.

9. The integrated circuit device of Claim 8 wherein one of said implantation regions is coupled to a first source contact.

10. The integrated circuit device of Claim 8 wherein one of said implantation regions is coupled to a common source line.

11. The integrated circuit device of Claim 8 further comprising a second gate, wherein a second region under said second gate comprises overlapping lateral diffusions of source and drain implantation regions.

12. The integrated circuit device of Claim 11 wherein one of said implantation regions associated with said second gate structure is coupled to a second source contact.

13. The integrated circuit device of Claim 11 wherein one of said implantation regions associated with said second gate structure is coupled to said common source line.

14. The integrated circuit device of Claim 8 further comprising non-volatile memory.

15. A method of manufacturing a source connection in an integrated circuit comprising:
forming gate structures of said integrated circuit;
implanting a source and a drain region of a desired Vss column;
coupling a source contact from a metal Vss line to said source region; and
laterally diffusing dopants of said source region to overlap dopants of said drain region.

16. The method as described in Claim 15 wherein said drain region is part of a common source line of said integrated circuit.

18. The method as described in Claim 15 wherein a portion of said gate structures form part of a word line of a non-volatile memory integrated circuit.

19. The method as described in Claim 18 wherein said gate structure comprises a floating gate for storing charge.

20. The method as described in Claim 18 wherein said word line is substantially straight.